CLAIMS

1. A method for programming a memory array, the method using programming pulses, the method comprising the step of:

adapting said programming pulses to the current state of said memory array.

2. A method according to claim 1 wherein said step of adapting includes the steps of:

determining the voltage level of the programming pulse used to program generally the fastest bit of said memory array; and

setting an initial programming pulse level of said memory array to a level in the general vicinity of said programming pulse level of said generally fastest bit.

3. A method according to claim 2 and wherein said step of determining includes the steps of:

programming a small set of bits of said memory array;

setting a starting programming pulse level to a programming pulse level not higher than the programming pulse level used to program a fast bit of said small set;

programming generally all of the bits of said memory array beginning at said starting programming pulse level; and

setting said initial programming pulse level to a programming pulse level in the general vicinity of a programming pulse level of a fast bit of generally all of said bits.

4. A method according to claim 1 wherein said general vicinity is not higher than said programming pulse level of said fast bit.

5. A method according to claim 3 wherein said generally all of the bits is all the bits of the array but the bits of said small set.

6. A method according to claim 3 wherein said generally all of the bits is all of the bits of said array.

7. A method according to claim 1 and wherein said step of adapting includes the steps of:

measuring the current threshold level of a bit to within a predetermined range; and

selecting an incremental voltage level of a next programming pulse for said bit in accordance with said measured current threshold level.

8. A method according to claim 7 and wherein said step of measuring includes the step of having multiple verify levels for said array.

9. A method according to claim 8 and wherein said step of measuring also includes the step of after a programming pulse, comparing a threshold level of a group of bits which have received said programming pulse to at least one of said verify levels and said step of selecting includes the step of selecting a next programming pulse level according to generally the highest verify level achieved by said group.

10. A method according to claim 9 and also comprising the steps of removing any bit which has been programmed from said group and repeating said steps of comparing and selecting until there are no more bits in said group.

11. A method according to claim 8 and wherein said step of measuring also includes the step of after a programming pulse, comparing a threshold level of a bit which received said programming pulse to at least one of said verify levels and said step of selecting includes the step of selecting a next programming pulse level according to generally the highest verify level achieved by said bit.

12. A method according to claim 7 and wherein the magnitude of said incremental voltage level corresponds to said measured current threshold level such that, after programming with said incremental voltage level, said bit generally is fully programmed.

13. A method according to claim 7 and wherein the magnitude of said incremental voltage level corresponds to said measured current threshold level such that, after programming with said incremental voltage level, said bit generally is slightly less than fully programmed.

14. A method according to claim 13 and also comprising the step of final programming said bit with a small incremental voltage level after said step of programming with said incremental voltage level.

15. A method for erasing a memory array, the method using erase pulses, the method comprising the step of:

adapting said erase pulses to the current state of said memory array.

16. A method according to claim 15 wherein said step of adapting includes the steps of:

determining erase conditions of the erase pulse used to erase a representative portion of said memory array; and

setting initial erase conditions of said memory array to the general vicinity of said erase conditions of said representative portion.

17. A method according to claim 15 and wherein said step of adapting includes the steps of:

measuring the current threshold level of a bit to within a predetermined range; and

selecting an incremental voltage level of a next erase pulse for said bit in accordance with said measured current threshold level.

18. A method according to claim 17 and wherein said step of measuring includes the step of having multiple verify levels for said array.

19. A method according to claim 17 and wherein said step of measuring also includes the step of after an erase pulse, comparing a threshold level of a group of bits which have received said erase pulse to at least one of said verify levels and said step of selecting includes the step of selecting a next erase pulse level according to generally the lowest verify level achieved by said group.

20. A method according to claim 19 and also comprising the steps of removing any bit which has been erased from said group and repeating said steps of comparing and selecting until there are no more bits in said group.

21. A method according to claim 17 and wherein said step of measuring also includes the step of after an erase pulse, comparing a threshold level of a bit which received said erase pulse to at least one of said verify levels and said step of setting includes the step of selecting a next erase pulse level according to generally the lowest verify level achieved by said bit.

22. A method according to claim 16 and wherein said erase conditions comprises at least one of the following set: the gate voltage level, the drain voltage level, the erase duration and any combination thereof.